

WHAT IS CLAIMED IS:

1 1. A phase-locked loop (PLL) frequency synthesizer
2 comprising:

3 a voltage controlled oscillator (VCO) that receives a
4 frequency control voltage level stored on a loop filter and
5 generates an output clock signal having an operating frequency,
6 F_{out} , determined by said frequency control voltage level;

7 a first frequency divider for dividing said operating
8 frequency, F_{out} , of said output clock signal by a first divider
9 value, N , to produce a first divided clock signal having a
10 frequency, F_{out}/N ;

11 a second frequency divider for dividing a reference
12 frequency, F_{in} , of an incoming reference clock signal by a second
13 divider value, M , to produce a second divided clock signal having
14 a frequency, F_{in}/M ;

15 a phase-frequency detector capable of comparing said
16 first and second divided clock signals and generating an UP
17 control signal if said first divided clock signal is slower than
18 said second divided clock signal and generating a DOWN control
19 signal if said first divided clock signal is faster than said
20 second divided clock signal;

21 a charge pump capable of receiving said UP and DOWN
22 control signals and increasing said frequency control voltage

23 level on said loop filter by injecting a charge pump current, I_c ,
24 and decreasing said frequency control voltage level on said loop
25 filter by draining said charge pump current, I_c ; and

26 a loop response control circuit capable of adjusting a
27 value of I_c as a function of said first divider value, N , and
28 said second divider value, M .

1 2. The phase-locked loop frequency synthesizer as set
2 forth in Claim 1 wherein said loop response control circuit, for
3 a given value of M , sets I_c to a minimum current level when N is
4 in the range $1 \leq N \leq K$ and sets I_c to a second current level
5 higher than said minimum current level when N is in the range
6 $K+1 \leq N \leq P$.

1 3. The phase-locked loop frequency synthesizer as set
2 forth in Claim 2 wherein said second current level is
3 approximately twice said minimum current level.

1 4. The phase-locked loop frequency synthesizer as set
2 forth in Claim 3 wherein said loop response control circuit sets
3 I_c to a third current level higher than said second current level
4 when N is in the range $P+1 \leq N \leq S$.

1 5. The phase-locked loop frequency synthesizer as set
2 forth in Claim 4 wherein said third current level is
3 approximately twice said second current level.

1 6. The phase-locked loop frequency synthesizer as set
2 forth in Claim 1 wherein said loop response control circuit, for
3 a given value of N, sets I_c to a maximum current level when M is
4 in the range $1 \leq M \leq J$ and sets I_c to a second current level
5 lower than said maximum current level when M is in the range
6 $K+1 \leq N \leq Q$.

1 7. The phase-locked loop frequency synthesizer as set
2 forth in Claim 6 wherein said second current level is
3 approximately one half of said maximum current level.

1 8. The phase-locked loop frequency synthesizer as set
2 forth in Claim 7 wherein said loop response control circuit sets
3 I_c to a third current level lower than said second current level
4 when M is in the range $Q+1 \leq N \leq T$.

1 9. The phase-locked loop frequency synthesizer as set
2 forth in Claim 8 wherein said third current level is
3 approximately one half of said second current level.

1 10. The phase-locked loop frequency synthesizer as set
2 forth in Claim 1 wherein said loop response control circuit is
3 further capable of adjusting a resistance, R, of a filter
4 resistor associated with said loop filter as a function of said
5 first divider value, N, and said second divider value, M.

1 11. The phase-locked loop frequency synthesizer as set
2 forth in Claim 10 wherein said loop response control circuit, for
3 a given value of N, sets R to a minimum resistance value when M
4 is in the range $1 \leq M \leq U$ and sets R to a second resistance level
5 higher than said minimum resistance level when M is in the range
6 $U+1 \leq M \leq V$.

1 12. The phase-locked loop frequency synthesizer as set
2 forth in Claim 11 wherein said second resistance level is
3 approximately twice said minimum resistance level.

1 13. The phase-locked loop frequency synthesizer as set
2 forth in Claim 12 wherein said loop response control circuit sets
3 R to a third resistance level higher than said second resistance
4 level when M is in the range $V+1 \leq M \leq W$.

1 14. The phase-locked loop frequency synthesizer as set
2 forth in Claim 13 wherein said third resistance level is
3 approximately twice said second resistance level.

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1 15. An integrated circuit comprising:

2 a processor capable of operating at a plurality of
3 clock speeds;

4 a phase-locked loop (PLL) frequency synthesizer capable
5 of providing at least one clock signal having a variable clock
6 speed to said processor, said PLL frequency synthesizer
7 comprising:

8 a voltage controlled oscillator (VCO) that
9 receives a frequency control voltage level stored on a loop
10 filter and generates an output clock signal having an
11 operating frequency, F_{out} , determined by said frequency
12 control voltage level;

13 a first frequency divider for dividing said
14 operating frequency, F_{out} , of said output clock signal by a
15 first divider value, N , to produce a first divided clock
16 signal having a frequency, F_{out}/N ;

17 a second frequency divider for dividing a
18 reference frequency, F_{in} , of an incoming reference clock
19 signal by a second divider value, M , to produce a second
20 divided clock signal having a frequency, F_{in}/M ;

21 a phase-frequency detector capable of comparing
22 said first and second divided clock signals and generating
23 an UP control signal if said first divided clock signal is
24 slower than said second divided clock signal and generating

25 a DOWN control signal if said first divided clock signal is
26 faster than said second divided clock signal;

27 a charge pump capable of receiving said UP and
28 DOWN control signals and increasing said frequency control
29 voltage level on said loop filter by injecting a charge
30 pump current, I_c , and decreasing said frequency control
31 voltage level on said loop filter by draining said charge
32 pump current, I_c ; and

33 a loop response control circuit capable of
34 adjusting a value of I_c as a function of said first divider
35 value, N , and said second divider value, M .

1 16. The integrated circuit as set forth in Claim 15 wherein
2 said loop response control circuit, for a given value of M , sets
3 I_c to a minimum current level when N is in the range $1 \leq N \leq K$
4 and sets I_c to a second current level higher than said minimum
5 current level when N is in the range $K+1 \leq N \leq P$.

1 17. The integrated circuit as set forth in Claim 16 wherein
2 said second current level is approximately twice said minimum
3 current level.

1 18. The integrated circuit as set forth in Claim 17 wherein
2 said loop response control circuit sets I_c to a third current
3 level higher than said second current level when N is in the
4 range $P+1 \leq N \leq S$.

1 19. The integrated circuit as set forth in Claim 18 wherein
2 said third current level is approximately twice said second
3 current level.

1 20. The integrated circuit as set forth in Claim 15 wherein
2 said loop response control circuit, for a given value of N , sets
3 I_c to a maximum current level when M is in the range $1 \leq M \leq J$
4 and sets I_c to a second current level lower than said maximum
5 current level when M is in the range $K+1 \leq N \leq Q$.

1 21. The integrated circuit as set forth in Claim 20 wherein
2 said second current level is approximately one half of said
3 maximum current level.

1 22. The integrated circuit as set forth in Claim 21 wherein
2 said loop response control circuit sets I_c to a third current
3 level lower than said second current level when M is in the range
4 $Q+1 \leq N \leq T$.

1 23. The integrated circuit as set forth in Claim 22 wherein
2 said third current level is approximately one half of said second
3 current level.

1 24. The integrated circuit as set forth in Claim 15 wherein
2 said loop response control circuit is further capable of
3 adjusting a resistance, R, of a filter resistor associated with
4 said loop filter as a function of said first divider value, N,
5 and said second divider value, M.

1 25. The integrated circuit as set forth in Claim 24 wherein
2 said loop response control circuit, for a given value of N, sets
3 R to a minimum resistance value when M is in the range $1 \leq M \leq U$
4 and sets R to a second resistance level higher than said minimum
5 resistance level when M is in the range $U+1 \leq M \leq V$.

1 26. The integrated circuit as set forth in Claim 25 wherein
2 said second resistance level is approximately twice said minimum
3 resistance level.

1 27. The integrated circuit as set forth in Claim 26 wherein
2 said loop response control circuit sets R to a third resistance
3 level higher than said second resistance level when M is in the
4 range $V+1 \leq M \leq W$.

1 28. The integrated circuit as set forth in Claim 27 wherein
2 said third resistance level is approximately twice said second
3 resistance level.

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